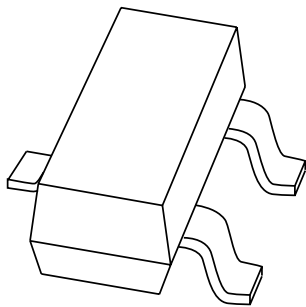


# DATA SHEET



## **PDTD114ET** NPN resistor-equipped transistor

Objective specification  
Supersedes data of February 1995  
File under Discrete Semiconductors, SC04

1997 Sep 02

# NPN resistor-equipped transistor

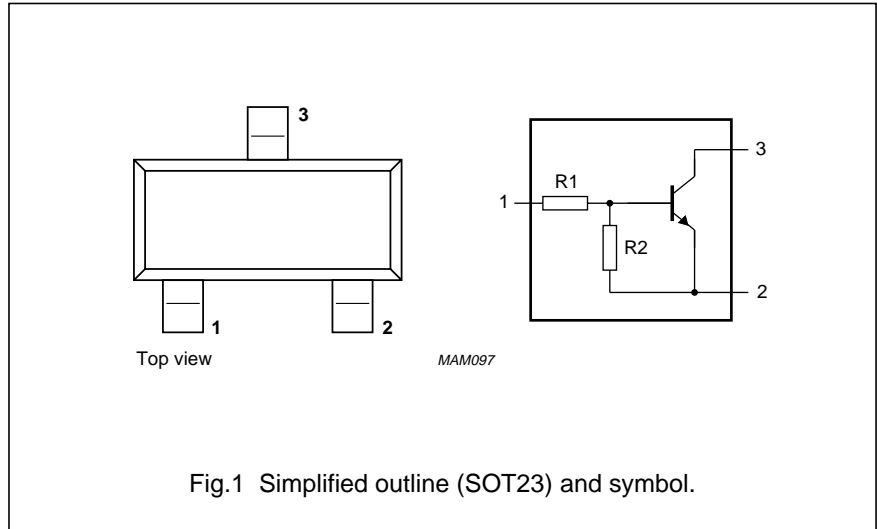
# PDTD114ET

### FEATURES

- Built-in bias resistors R1 and R2 (typ. 10 kΩ each)
- Simplification of circuit design
- Reduces number of components and board space.

### APPLICATIONS

- Especially suitable for space reduction in interface and driver circuits
- Inverter circuit configurations without use of external resistors.

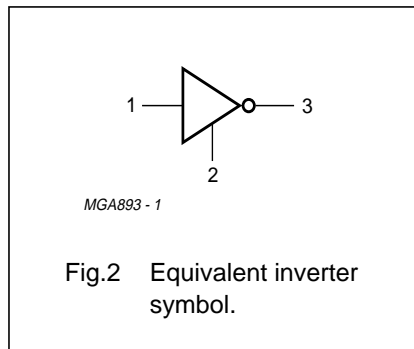


### DESCRIPTION

NPN resistor-equipped transistor in a SOT23 plastic package.  
 PNP complement: PDTB114ET.

### PINNING

PIN	DESCRIPTION
1	base/input
2	emitter/ground
3	collector/output



### MARKING

TYPE NUMBER	MARKING CODE
PDTD114ET	p10

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CE0}$	collector-emitter voltage	open base	–	–	50	V
$I_O$	output current (DC)		–	–	500	mA
$I_{CM}$	peak collector current		–	–	500	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$	–	–	250	mW
$h_{FE}$	DC current gain	$I_C = 50\text{ mA}; V_{CE} = 5\text{ V}$	56	–	–	
R1	input resistor		7	10	13	kΩ
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	

## NPN resistor-equipped transistor

## PDTD114ET

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CBO</sub>	collector-base voltage	open emitter	–	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	10	V
V <sub>I</sub>	input voltage				
	positive		–	+40	V
	negative		–	–10	V
I <sub>O</sub>	output current (DC)		–	500	mA
I <sub>CM</sub>	peak collector current		–	500	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	250	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C

**Note**

1. Transistor mounted on an FR4 printed-circuit board.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	note 1	500	K/W

**Note**

1. Transistor mounted on an FR4 printed-circuit board.

## NPN resistor-equipped transistor

## PDTD114ET

**CHARACTERISTICS**

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CBO}$	collector cut-off current	$I_E = 0; V_{CB} = 50\text{ V}$	–	–	100	nA
$I_{CEO}$	collector-emitter cut-off current	$I_B = 0; V_{CE} = 30\text{ V}$	–	–	1	$\mu\text{A}$
		$I_B = 0; V_{CE} = 30\text{ V}; T_j = 150\text{ °C}$	–	–	50	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$I_C = 0; V_{EB} = 5\text{ V}$	–	–	500	$\mu\text{A}$
$h_{FE}$	DC current gain	$I_C = 50\text{ mA}; V_{CE} = 5\text{ V};$ note 1	56	–	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 50\text{ mA}; I_B = 2.5\text{ mA};$ note 1	–	–	300	mV
$V_{i(off)}$	input off voltage	$I_C = 100\text{ }\mu\text{A}; V_{CE} = 5\text{ V}$	–	–	500	mV
$V_{i(on)}$	input on voltage	$I_C = 10\text{ mA}; V_{CE} = 300\text{ mV}$	3	–	–	V
R1	input resistor		7	10	13	$\text{k}\Omega$
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
$C_c$	collector capacitance	$I_E = i_e = 0; V_{CB} = 10\text{ V}; f = 1\text{ MHz}$	–	–	8	pF

**Note**

1. Pulse test:  $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02.$

NPN resistor-equipped transistor

PDTD114ET

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT23



## NPN resistor-equipped transistor

PDTD114ET

**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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NPN resistor-equipped transistor

PDTD114ET

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